Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **D1**
2. **D3**
3. **S3**
4. **S4**
5. **D4**
6. **D2**
7. **S2**
8. **A2**
9. **V+**
10. **VL**
11. **VR**
12. **V-**
13. **A1**
14. **S1**

**.081”**

**1 14 13**

**6 7 8**

**12**

**11**

**10**

**9**

**2**

**3**

**4**

**5**

**HI**

**5051**

**MASK**

**REF**

**.096”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: V- or FLOAT**

**Mask Ref: HI 5051**

**APPROVED BY: DK DIE SIZE .081” X .096” DATE: 8/25/21**

**MFG: HARRIS / INTERSIL THICKNESS .025” P/N: HI0-5051**

**DG 10.1.2**

#### Rev B, 7/1